## CLAIMS

What is claimed is:

1.     A test system for measuring the response time of a squelch detection
circuit configured to detect a squelch state over a differential signal pair, the
differential signal pair having a first signal line and a second signal line, the test
system comprising:

a signal generator configured to drive a first square wave onto the first signal
line and a second square wave onto the second signal line, the frequency of the first
signal line being higher than the frequency of the second signal line, the amplitudes of
the first and second square waves being essentially equal;

a clock generator configured to produce a clock signal of a higher frequency
than the first square wave; and

a pulse counter configured to count the number of pulses of the clock signal,
and the number of pulses of the clock signal that occur while a squelch detect signal
of the squelch detection circuit is active.

2.     The test system of claim 1, wherein the frequencies of the first square
wave and the second square wave may be varied.

3.     The test system of claim 1, wherein the phase between the first square
wave and the second square wave may be varied.

4.     The test system of claim 1, wherein the signal generator is a waveform
generator.

5.      The test system of claim 1, wherein the signal generator is a pulse

2    generator.


6.      A method for measuring the response time of a squelch detection

2    circuit configured to detect a squelch state over a differential signal pair, the

differential signal pair having a first signal line and a second signal line, the method

4    comprising:

driving the first signal line with a first square wave having a period twice the

6    duration of a squelch state that is essentially always detectable by the squelch

detection circuit;

8            driving the second signal line with a second square wave having a period that

is an integral multiple of the period of the first square wave, the period of the second

10   square wave being at least four times the period of the first square wave, the second

square wave being in phase with, and having essentially the same amplitude as, the

12   first square wave;

gradually reducing the period of both the first and second square waves by the

14   same percentage until the duty cycle of a squelch detect signal of the squelch

detection circuit is less than fifty percent, resulting in a final period of the first square

16   wave; and

calculating the response time of the squelch detection circuit as half of the

18   final period of the first square wave.


7.      The method of claim 6, further comprising verifying that the duty

2    cycle of the squelch detect signal of the squelch detection circuit is approximately

fifty percent prior to the gradually reducing step.


8.      The method of claim 6, wherein the first square wave and the second

2    square wave are generated by a signal generator.


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9.      The method of claim 6, wherein the number of pulses of a clock signal,

2    and the number of pulses of the clock signal that occur while the squelch detect signal

of the squelch detection circuit is active, are counted by a pulse counter to determine

4    the duty cycle of the squelch detect signal.

10.    The method of claim 9, wherein the number of pulses of the clock

2    signal that occur during a cycle of the first square wave is at least 200.

11.    The method of claim 9, wherein the duty cycle of the squelch detect

2    signal of the squelch detection circuit is measured by the pulse counter over at least

16 cycles of the second square wave.

12.    A method for measuring the response time of a squelch detection

2    circuit configured to detect a squelch state over a differential signal pair, the

differential signal pair having a first signal line and a second signal line, the method

4    comprising:

driving the first signal line with a first square wave having a period four times

6    the duration of a squelch state that is essentially always detectable by the squelch

detection circuit;

8    driving the second signal line with a second square wave having a period that

is an integral multiple of the period of the first square wave, the period of the second

10    square wave being at least four times the period of the first square wave, the second

square wave lagging the first square wave by ninety degrees, the second square wave

12    having essentially the same amplitude as the first square wave;

gradually increasing the phase lag of the second square wave compared to the

14    first square wave until the duty cycle of a squelch detect signal of the squelch

detection circuit is less than fifty percent, resulting in a final phase lag of the second

16    square wave; and

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calculating the response time of the squelch detection circuit as 180 degrees

18    minus the final phase lag of the second square wave, divided by 360 degrees,

multiplied by the period of the first square wave.

13.    The method of claim 12, further comprising verifying that the duty

2    cycle of the squelch detect signal of the squelch detection circuit is approximately

fifty percent prior to the gradually increasing step.

14.    The method of claim 12, wherein the first square wave and the second

2    square wave are generated by a signal generator.

15.    The method of claim 12, wherein the number of pulses of a clock

2    signal, and the number of pulses of the clock signal that occur while the squelch

detect signal of the squelch detection circuit is active, are counted by a pulse counter

4    to determine the duty cycle of the squelch detect signal.

16.    The method of claim 15, wherein the number of pulses of the clock

2    signal that occur during a cycle of the first square wave is at least 200.

17.    The method of claim 15, wherein the duty cycle of the squelch detect

2    signal of the squelch detection circuit is measured by the pulse counter over at least

16 cycles of the second square wave.

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